Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (original) An apparatus comprising:

a task table coupled to a bus interface to store task entries corresponding to tasks executed by at least one processor;

a block allocation circuit coupled to the bus interface and a cache memory to allocate blocks of the cache memory used by at least one of the tasks; and

a task coordinator to coordinate the tasks in response to a task cycle issued by the at least one processor.

2. (original) The apparatus of claim 1 wherein each of the task entries comprises at least one of a task status, a task identifier (ID), a task start address, a task block size, and a task cache address.

3. (original) The apparatus of claim 2 wherein the task cycle provides at least one of the task ID, a task command, the task start address, and the task block size.

4. (original) The apparatus of claim 3 wherein the block allocation circuit comprises:

a search logic circuit to locate a free block by shifting through a list of busy flags corresponding to data blocks in use in the cache memory; and

a block information generator coupled to the block search logic to generate block information of a free block available for a new task, the block information including at least a block size, a block starting address, and a block ending address.

5. (original) The apparatus of claim 1 wherein the task coordinator comprises:

a task table updater to update the task table; and

an address generator to generate address information to the cache memory.

6. (original) The apparatus of claim 3 wherein the task status is one of an invalid status, a shared status, and an exclusive status.

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7. (original) The apparatus of claim 6 wherein the task command is one of a read shared command, a read exclusive command, a write command, and a flush command.

8. (original) The apparatus of claim 7 wherein the task block size corresponds to number of cache lines in one of the blocks.

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9. (original) The apparatus of claim 8 wherein the bus interface is one of a processor bus interface and a multiprocessor bus interface.

10. (original) The apparatus of claim 9 wherein the cache memory is one of an internal cache and an external cache with respect to the at least one processor.

11. (original) A method comprising:

storing task entries corresponding to tasks executed by at least one processor in a task table;

allocating blocks of the cache memory used by at least one of the tasks; and

coordinating the tasks in response to a task cycle issued by the at least one processor.

12. (original) The method of claim 11 wherein each of the task entries comprises at least one of a task status, a task identifier (ID), a task start address, a task block size, and a task cache address.

13. (original) The method of claim 12 wherein the task cycle provides at least one of the task ID, a task command, the task start address, and the task block size.

14. (original) The method of claim 13 wherein allocating comprises:

locating a free block by shifting through a list of busy flags corresponding to data blocks in use in the cache memory; and

generating block information of a free block available for a new task, the block information including at least a block size, a block starting address, and a block ending address.

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15. (original) The method of claim 11 wherein coordinating the tasks comprises:

updating the task table; and

generating address information to the cache memory.

16. (original) The method of claim 13 wherein the task status is one of an invalid status, a shared status, and an exclusive status.

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17. (original) The method of claim 16 wherein the task command is one of a read shared command, a read exclusive command, a write command, and a flush command.

18. (original) The method of claim 17 wherein the task block size corresponds to number of cache lines in one of the blocks.

19. (original) The method of claim 18 wherein the bus interface is one of a processor bus interface and a multiprocessor bus interface.

20. (original) The method of claim 19 wherein the cache memory is one of an internal cache and an external cache with respect to the at least one processor.

21. (original) A system comprising:

a processor bus; and

a plurality of processors coupled to the processor bus, each of the plurality of processors having an internal task manager and an internal cache memory, the internal task manager comprising:

a task table coupled to a bus interface to store task entries corresponding to tasks executed by at least one processor,

a block allocation circuit coupled to an internal bus interface and the interval cache memory to allocate blocks of the interval cache memory used by at least one of the tasks, and

a task coordinator to coordinate the tasks in response to a task cycle issued by the at least one processor.

22. (original) The system of claim 21 wherein each of the task entries comprises at least one of a task status, a task identifier (ID), a task start address, a task block size, and a task cache address.

23. (original) The system of claim 22 wherein the task cycle provides at least one of the task ID, a task command, the task start address, and the task block size.

24. (original) The system of claim 23 wherein the block allocation circuit comprises:

a search logic circuit to locate a free block by shifting through a list of busy flags corresponding to data blocks in use in the internal cache memory; and

a block information generator coupled to the block search logic to generate block information of a free block available for a new task, the block information including at least a block size, a block starting address, and a block ending address.

25. (original) The system of claim 21 wherein the task manager comprises:

a task table updater to update the task table; and

an address generator to generate address information to the interval cache memory.

26. (original) The system of claim 23 wherein the task status is one of an invalid status, a shared status, and an exclusive status.

27. (original) The system of claim 26 wherein the task command is one of a read shared command, a read exclusive command, a write command, and a flush command.

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28. (original) The system of claim 27 wherein the task block size corresponds to number of cache lines in one of the blocks.

29. (original) The system of claim 28 wherein the processor bus is a multiprocessor bus.

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30. (original) The system of claim 9 further comprising:

a external cache memory; and

an external task manager coupled to the external cache memory and the processor bus, the external task manager comprising:

an external task table to store task entries corresponding to tasks executed by at least one processor,

a external block allocation circuit coupled to the processor bus and the external cache memory to allocate blocks of the external cache memory used by the tasks, and

an external task coordinator to coordinate the tasks in response to the task cycle issued by the at least one processor.